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09/998,848	11/15/2001	Kenneth Y. Ogami	CD01177M	6884

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CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
VO, TED T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/998,848	OGAMI, KENNETH Y.	
	Examiner	Art Unit	
	TED T. VO	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16,26-30 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16, 26-30, 36-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Eight separate copies of IDS's filed on 1/29/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 02/24/2009.

Claims 1-14, 16, 26-30, 36-38 are pending in this application.

Information Disclosure Statement

2. The citations in the PTO-1449 forms, filed on 01/29/2009, which are the information of internal office actions issued by Examiners will be **considered**, but not be initialed. Any cited reference when initialed will appear in a printed patent if an application is allowed; therefore, it will be improper to name an internal office action in its printed patent. Moreover, a cited information in NPL section presents a prior art. By citing it, it could be used by the examiner for a rejection. Therefore, Applicant should cite only a related **application serial number or application publication, instead of citing its internal office action**.

Response to Arguments

3. Applicants' arguments in the Remarks section filed on 02/24/2009 have been respectfully considered, but are moot in view of the new amendment.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites said first and said second markup language fail to be sufficient antecedent basis in the claim. It appears the claim is dependent on claim 37, instead. Correction is required.

Claim Rejections - 35 USC § 103

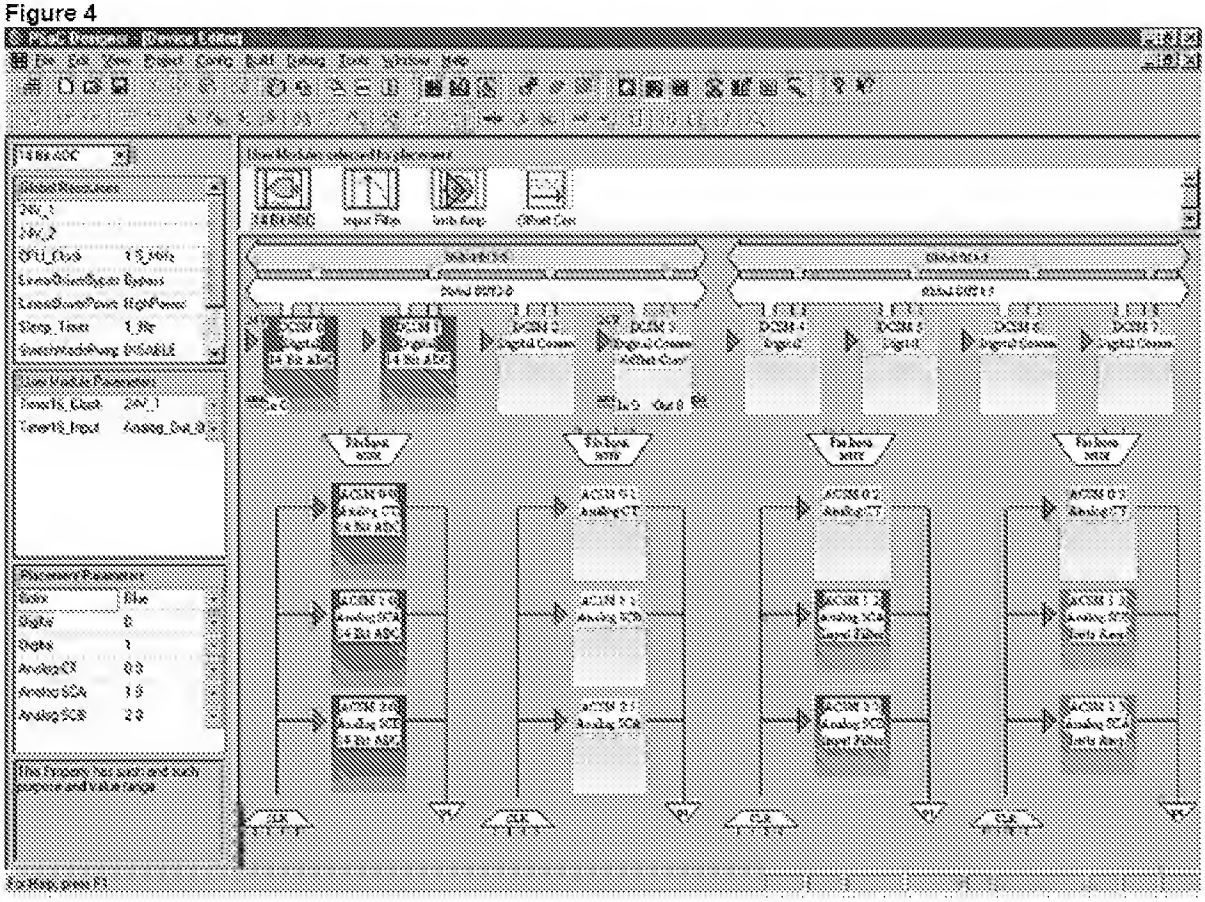
6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-14, 16, 26-30, 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra, "Programmable SoC Delivers A New Level Of System Flexibility", 2000, in view of Hamblen, "Rapid Prototyping using Field Programmable logic Devices", 6-2000.

As per Claim 1: Bindra discloses

Figure 4



4. The PSoC Designer is an integral part of the Windows-based development process. Its device editor employs a graphical interface to connect user modules, which are next mapped onto the SoCblocs on-chip. Finally, the user selects the pin assignments.

Which includes displaying a collection of virtual blocks in a design system, each virtual block (i.e. a block in main pane) is a programmable block that is selected from the top pane for embedding to the collection for forming a project. With a user module being connected to a virtual block, configured by corresponding information provided in the left pane, it forms a user module presenting the functional circuit of a virtual block. The figure 1 appears a building block that is embedded within the collection because it contains input/output pins connecting to another virtual block; and thus, if depict a selected block such as a module of Figure 1 or another simpler block, it will provide a user to construct the code module representing the function of the depicted block. It appears covers the limitations recited within:

A method for configuring a microcontroller, comprising:

displaying a first graphical user interface <u>on a display device of a computer system,</u> <u>said first graphical user interface</u> comprising a collection of virtual blocks in a design system (see figure 4);

receiving <u>at said computer system</u> a selection of a user module, wherein said user module comprises information for implementing a function using a programmable physical block (Figure 4, selecting a 14 Bit ADC, part of Library modules or user modules (p. 3, include line 5));

displaying <u>on said display device</u> a second graphical user interface operable for receiving user-specifiable information about said user module (Figure 4, selecting a 14 Bit ADC as a virtual block, and its module (p. 3) provided with user input parameters in the left area of the PSoC Designer)***;***

assigning a virtual block taken from said collection to said user module, wherein said virtual block corresponds to said programmable physical block (Figure 4, selecting a 14 Bit ADC, part of Library modules or user modules (p.3), and take the input parameters assigned by user into the module)***; and***

constructing completely computer-generated source code that is loaded into a register of said programmable physical block to cause said programmable physical block to implement said function

Bindra shows each user module is designed by user code to present the function of that module. The function is represented by source code (user module) to cause its programmable physical block to implement the function. It does not show the source code is loaded or constructed to implement.

It should be noted that every source code that implement a virtual block is an executable code such as assembly language. There is no thing new for this.

Hamblen shows a programmable on chip design process (p. 36, Figure 11) using a CAD tool that takes design virtual blocks and constructs source code. The source code in form assemble or machine language that is automatically generated by a C compiler to mapped on to the Virtual blocks designed from the CAD tool (See Figure 1: VHDL Design entity (i.e. Virtual blocks) connected with automatically generated code generated by a C Compiler, mapped to virtual blocks at gate levels in the CAD tool) for obviously disclosing: "*automatically constructing source code*"

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to know that, for an enablement, it requires every module in the PSoC

Designer discussed by Bindra is automatically generated into executable "code", and **automatically connected** to a corresponding virtual block when a circuit is built in the system by a PSoc Designer, shown by Bindra. It is obvious because, in order to present a functionality of a circuit, a user can manually program a circuit in an assembly program with assigned parameters presenting element configuration (i.e. a source code that represents for a circuit); but it will **take days** for him to do so. For conforming to the availability of source code generation, tools and compiler is available for use at that time, thus it will generate automatically into assemble code and/or machine code for manual acts, as shown by Hamblen in Figure 11.

As per Claim 2: Bindra further discloses,

The method of Claim 1, wherein said function comprises a pulse width modulator (Bindra: See Figure 4, "User Module" that represents various Digital functions, and see P.2 line 36, "PWMs").

As per Claim 3: Bindra further discloses, *The method of Claim 1, wherein said function comprises a timer.* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36, "*timers*").

As per Claim 4: Bindra further discloses, *The method of Claim 1, wherein said function comprises an analog-to-digital converter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35, "ADCs").

As per Claim 5: Bindra further discloses, *The method of Claim 1, wherein said function comprises a digital-to-analog converter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35 "DACs").

As per Claim 6: Bindra further discloses, *The method of Claim 1, wherein said function comprises a counter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36 "counters").

As per Claim 7: Bindra further discloses, *The method of Claim 1, wherein said function comprises a signal amplifier.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 33 *"differential amplifiers"*).

As per Claim 8: Bindra further discloses, *The method of Claim 1, wherein said function provides serial communication.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.3, line 9, "serial transmitters/receivers").

As per Claim 9: Bindra further discloses, *The method of Claim 1, wherein said collection is displayed as a two dimensional array of programmable analog virtual blocks and programmable digital virtual blocks.* (See collections in the right bottom section, which is *two-dimensional array*).

As per Claim 10: Bindra further discloses, *The method of Claim 1, wherein said assigning further comprises assigning a second virtual block to said user module* (See collections in the right bottom section, which is two *dimensional array*).

As per Claim 11: Bindra further discloses, *The method of Claim 1, wherein said source code comprises a symbolic name for a register address in said programmable physical block.* (Bindra: See page 2, lines 12-17 ('register space that holds the configuration information').

As per Claim 12: Bindra further discloses, *The method of Claim 11 wherein said symbolic name is derived from said function.* (See Bindra 'User module" in Figure 4, where user module

represents a circuit element. Each circuit element is a symbolic name function: e.g.: ADC, DAC, Timer, Counter, etc).

As per Claim 37: Bindra further discloses, *The method of Claim 1 wherein said user module is represented by first markup language data that includes information defining how configuration register for said microcontroller are be programmed in order to implement said function, and wherein said programmable physical is represented by second markup data that includes information defining physical addresses of said configuration registers.*

Official notice is taken that Markup language such as SGML, HTML, XML, is the language that is provided computer rendering. There is no invention on using the markup language for rendering, but compliant to the rules set forth by the language. This is well known, The Figure 4 of Bindra can be implemented by XML and its data, and the use of Markup languages is only to take the advantage of the availability that is designed for graphical rendering (The well-known HTML and XML is available in the Internet, Example, Applicants can refer to the website XML.com).

Therefore, it is obvious for an ordinary in the art when something like mark up language become standard for providing the graphical rendering; one will take the advantage to use it by including it for conforming to the availability.

As per Claim 36: Incorporated to the rejection of claim 1, Bindra and Hamblen further discloses

The method of Claim 1 wherein said automatically constructing source code comprises:

linking said first markup language data and said second markup language data;

reading template files; substituting said user-specifiable comprising information specific to said user module, information specific to said function and information specific to a control parameter of said function for generic information in said template files to produce assembly, include and

header files; compiling said assembly, include and header files to produce an executable file; downloading said executable file as a code block to a memory of said microcontroller; and executing said code block to configure said programmable block.

as in the Figures 7, 9-11 (Hamblen). It is obvious, because the claimed recitation conforms to or complies with basis process of C compiler when it generates assembly language; i.e. a C program has "include statements", or "header files"; therefore, every template created from the C compiler for an assembly program will include with "header files" such #include statement on its top. It is obvious because it is conforming to a C program → assembly program.

Bindra and Hamblen further in combined fail to disclose a very well-known markup language, that is usually available for graphical rendering; where the Markup language is usable for rendering virtual blocks such as the blocks shown in Figure 4.

Official notice is taken: the obviousness is as addressed as set forth in the rejection in the claim 37.

As per Claim 13: See the rationale addressed in Claim 1.

As per Claim 14: Regarding,

"The method of Claim 13, wherein said automatically constructing further comprises:

computing a register address for a register within said programmable physical block; determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design; and substituting said symbolic name for a generic name in said template assembly code". See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish');

- *computing a register address for a register within said programmable block:* page 6, lines 7-13, referring "register mapping"

- *determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design:* page 2, lines 12-17, referring "holds the configuration information".

- *substituting said symbolic name for a generic name in said template assembly code:* referring the code construction performed by the PSoC Designer.

As per Claim 16: regarding limitations of Claim 16.

See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') for

- *determining a symbolic name corresponding to said user module and said circuit design;* referring "holds the configuration information".

- *computing a register address for a register within said programmable block;* referring "register mapping"

- *assigning said symbolic name to said register address; and placing said symbolic name into said assembly code in place of a generic name provided in said template assembly code file:* referring the code construction performed by the PSoC Designer.

As per claim 38: Regarding the limitation of claim 38. See the rationale addressed in the claims 36-37 above.

As per Claim 26: Regarding the limitation of claim 26, see the rationale addressed in the claims 1 and 36-37 above.

As per Claim 27: Regarding limitation, "The computer system of Claim 26, wherein said collection is displayed as a two dimensional array", see collection in the right bottom section of Figure 4.

As per Claim 28: Regarding limitation, *The computer system of Claim 26, wherein said assigning further comprises assigning a second virtual block to said user module*, it is either one of other blocks shown the right bottom section of Figure 4.

As per Claim 29: Regarding limitation, *The computer system of Claim 26, wherein said assembly code further comprises a symbolic name for a register address in said programmable physical block*, it is the code generated by the PSoC Design to the collection shown in the right

bottom section of Figure 4, where the symbolic name for a register address is done by register mapping as addressed above.

As per Claim 30: Regarding limitation, *The computer system of claim 26 wherein said symbolic name is derived from said function*, it is functionalized to a circuit element, and based on pins assignment to the user module.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
April 30, 2009

/Ted T. Vo/
Primary Examiner, Art Unit 2191